24. (Newly Added) A semiconductor device as recited in claim 23, wherein said another semiconductor device has electrodes that are connected to said wiring of the semiconductor device.

25. (Newly Added) A semiconductor device as recited in claim 19, wherein the semiconductor device is mounted on another semiconductor device with said confronting surface as a contacting surface, and said another semiconductor device has electrodes that are connected to said wiring and to at least one of said plurality of electrodes.

26. (Newly Added) A semiconductor device as recited in claim 23, wherein said another semiconductor device is disposed over a plurality of other semiconductor devices.

27. (Newly Added) A semiconductor device as recited in claim 18, wherein at least a part of said ball electrode is disposed on said wiring disposed on said side surface of said semiconductor element.

REMARKS

Amendments to the Specification and Proposed Corrections to the Drawings

Upon entry of the present amendment, newly presented claims 18-27 are pending, with claim 18 being the independent claim. Claims 9-17 have been withdrawn from consideration, and claims 1-8 have been canceled.

The proposed amendments to the drawings handwritten in red ink are believed to overcome the objections raised in the Office Action. Upon approval of the proposed changes, formal drawings will be submitted including the changes. With particular regard to the objections set forth in item 5 of page 2 of the Office Action, it is believed that the amendment to paragraph 2 of page 2 of the specification and the addition of reference

numeral '614' in proposed drawing Fig. 23(a) cures any defect. However, if there is further correction required, the Examiner is kindly requested to contact the undersigned attorney so that such issues may be addressed.

The amendment to the specification is submitted to overcome objections thereto as recited in the Office Action, while adding no new matter. This includes the amendments to the body of the specification as well as to the Title. Entry of these amendments is respectfully solicited.

In summary, it is believed that all objections set forth in items 2-8 and 10 of the Office Action are believed to have been addressed in the present response.

Response to Rejections Under 35 USC § 112, 102 and 103

The rejections under 35 USC § 112, second paragraph, are believed to be moot in view of the cancellation of claims 1-8, and the submission of newly added claims 18-27. However, it is respectfully submitted that the term 'confronting surface' as set forth in the newly added claims is well defined in its presentation in the application as filed. (Please refer, for example, to page 9, lines 25-26 of the application as filed). As such, it is respectfully submitted that this claimed element is in compliance with the referenced section of the United States Code, and it is respectfully submitted that this rejection be withdrawn.

The newly added claims are believed to be allowable over the prior art for at least the following reasons.

In order to properly establish a prima facie case of anticipation or obviousness, it is required that ***all*** of the claimed elements be disclosed in the applied art. Moreover, a prima facie case of anticipation requires that a single reference teaches as such elements; and a prima facie case of anticipation requires that a suitable motivation be

Conclusion

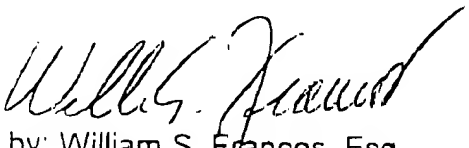
For at least the reasons set forth above claims 18-27 are believed to be allowable over the applied art. Allowance thereof is earnestly solicited.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact William S. Francos, Esq. (Reg. No. 38,456) at (610) 375-3513 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted on behalf of:

Oki Electric Industry Co., Ltd.



by: William S. Francos, Esq.

Registration No. 38,456

VOLENTINE FRANCOS, P.L.L.C.

WSF:mw

VOLENTINE FRANCOS, P.L.L.C.

12200 Sunrise Valley Drive, Suite 150

Reston, Virginia 20191

Telephone No.: (703) 715-0870

Facsimile No.: (703) 715-0877

provided for combining references. In either event, it follows that if a ***single*** element is neither taught nor suggested in the applied art, a prima facie case of anticipation or obviousness can be established.

Newly added claim 18 recites the limitations:

"...a semiconductor element having a circuit forming surface;

...and; a sealed confronting surface of said circuit forming surface."

For example, in an embodiment of the invention, the confronting surface (the back side) of the circuit forming surface is sealed allowing the semiconductor device of the embodiment to be mounted to another semiconductor device without shorting. (Please refer to the ultimate paragraph of page 14 of the application as filed for details).

It is respectfully asserted that this limitation is neither taught nor suggested by Applicants' admitted prior art (hereinafter 'APA'). To this end, the APA only teaches a semiconductor element 601 but fails to teach a sealed confronting surface. As such, *at the very least*, the applied art fails to teach this claimed limitation. Accordingly, because the applied art fails to teach at least one of the elements of the claimed invention, it cannot serve to establish a prima facie case of anticipation under 35 USC § 102. Moreover, because at least this limitation is neither taught nor suggested in the reference to Hatano, et al. (U.S. 6,104,088), the reference taken together lack the teaching of at least one of the claimed elements. Therefore, the applied art cannot properly establish a prima facie case of obviousness under 35 USC § 103.

It is respectfully submitted therefore that newly added claims 18-27 define over the applied art, and therefore, are allowable thereover. Allowance is earnestly solicited.

I. Marked Up Version of Title

[Semiconductor device, manufacturing method of semiconductor device, stack type semiconductor device, and manufacturing method of stack type semiconductor device] A SEMICONDUCTOR DEVICE HAVING A SEALED BACK SIDE

II. Marked-Up Version of Amended Paragraphs of the Specification

1. Second Paragraph of Page 2

A manufacturing method of such conventional semiconductor device is explained by referring to [Fig. 23] Figs. 23(a) - 23(e) and [Fig. 24] Figs. 24(a) and 24(e). [Fig. 23] Figs. 23(a)-23(e) are [is a] process sectional views showing a manufacturing method of the conventional semiconductor device. [Fig. 24] Figs. 24(a) - 24(e) are [is a] process sectional views showing the manufacturing method of the conventional semiconductor device.

2. Paragraphs on Page 7

[Fig.5] Figs. 5(a) - 5(f) is a flowchart showing the manufacturing process of the semiconductor element in the first embodiment.

[Fig.6] Fig. 6(a) - 6(f) is a flowchart showing the manufacturing process of the semiconductor element in the first embodiment.

[Fig. 7] Figs. 7(a) - 7(c) is a flowchart showing the manufacturing process of the semiconductor element in the first embodiment.

3. Paragraphs on Page 8

[Fig. 15] Figs. 15(a) - 15(e) is a flowchart showing the manufacturing process of the semiconductor element in the second embodiment.

[Fig. 23] Figs. 23(a) - 23 (e) are [is a] process sectional views for explaining the manufacturing method of the conventional semiconductor device.

[Fig. 24] Figs. 24(a) - 24 (e) are [is a] process sectional views for explaining the manufacturing method of the conventional semiconductor semiconductor device.

[Fig. 25] Figs. 25(a) - 25(c) are [is a] explanatory diagrams showing a configuration of a conventional semiconductor device mounting plural semiconductor elements.

4. Paragraph on Page 9

As shown in Fig. 1 and Fig. 2, in the semiconductor device of the embodiment, electrode pads 106 made of, for example, Al electrodes, are formed on a circuit forming surface (upper side in the drawing) of a semiconductor element 101, and, for example, a Cu wiring (re-wiring hereinafter) 104 is formed so as to be connected electrically to the electrode pads 106. Further, the Cu re-wiring 104 is connected electrically to Cu posts (bump electrodes) 102 of a height of , for example, about 100 μm. The circuit forming surface of the semiconductor element 101 is sealed by a resin 105 [to] exposing the surface

of the Cu posts 102. On the exposed surface of the Cu posts 102, for example, metal electrodes (ball electrodes) such as solder ball 103 are formed. On the confronting surface (back side) of the semiconductor element 101, on the other hand, the entire surface including the end portion of the Cu re-wiring 104 formed at the side surface is sealed with resin.

5. Paragraph on Page 10

In this embodiment, a part of the re-wiring 104 is formed at the side surface of the semiconductor element 101, while the back side of the semiconductor element 101 is sealed with the resin. Thus, the electrode terminal portion can be easily connected to the electrodes of other semiconductor devices across the resin 105 (for example, a thickness of about 50 μm) at the back side of the semiconductor element 101. As a result, plural semiconductor devices can be connected in a longitudinal profile, so that a stack type semiconductor device of high density mounting is realized without increasing the area.

6. Paragraph 2 on Page 12

[Consequently, as] As shown in Fig. 6 (a), the circuit forming surface of the semiconductor element 101 is sealed with the resin 105 so that it may be at least higher than the Cu post 102. As shown in Fig. 6 (b), a polisher 107 [grinding] polishes the resin 105 formed on the circuit forming surface of the semiconductor element 101, the surface of the Cu post 102 is exposed.

7. Paragraph 3 on Page 12

Then, as shown in Fig. 6 (c), [grinding] the polisher 107 is used for polishing the confronting surface (back side) of the circuit forming surface of the semiconductor wafer, the nearly concave groove 120 is exposed. Next, as shown in Fig. 6 (d), the back side of the semiconductor wafer is entirely sealed with the resin.

8. First Paragraph on Page 18

First, as shown in Fig. 15 (a), the circuit forming surface of the semiconductor element 301 is sealed with the resin 305 so as to be at least as high as or higher than the Cu post 302. Next, as shown in Fig. 15 (b), by polishing the resin 305 formed on the circuit forming surface of the semiconductor element 301 with polisher 307 the surface of the Cu post 302 is exposed.

9. Third Paragraph on Page 21

On the ball electrodes [203] of the conventional other semiconductor device, the semiconductor device of the embodiment is mounted, with its back side as the contact surface, so that the Cu re-wiring 104 and Cu posts 103 formed at the side surface of the semiconductor device of the first embodiment may be formed at nearly same positions, and is electrically connected to the electrodes of the other conventional semiconductor device through the solder balls 103. The solder balls 103 contact solder balls 215 disposed on electrode pad 213.

10. Ultimate Paragraph on Page 22

On the ball electrodes [403] of the conventional other semiconductor device, the semiconductor device of the second embodiment is mounted, with its back side as the contact surface, so that the Cu re-wiring 304 and Cu posts [303] 302 formed at the side

surface of the semiconductor device of the second embodiment may be formed at nearly same positions, and is electrically connected to the electrodes of the other conventional semiconductor device through the solder balls 303[.], which connect to solder balls 415 disposed on electrode pad 413.

Marked Up Version of the Abstract of the Disclosure

A semiconductor device capable mounting semiconductor elements having different functions without increasing the area of the semiconductor device, and its manufacturing method are presented. A part of wiring 104 is [al so] formed at the side surface of a semiconductor element 101, and bump electrodes 102 are formed so as to be nearly on a same plane as the wiring 104 formed at the side surface of the semiconductor element 101[.]. [at] At least a part of ball electrodes 103 is formed so as to connect electrically to the wiring 104 at the side surface of the semiconductor element, the side surface of the semiconductor element is sealed with resin exposing the wiring 104, and the confronting surface of the circuit forming surface is sealed with resin.